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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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MINNEAPOLIS, MN 55440-1022

EXAMINER	
ALROBAYE, IDRISS N	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,454	BUDNY ET AL.	
	Examiner	Art Unit	
	Idriss N. Alrobaye	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to communications through the applicant's application received on 02/01/2007.

2. Claims 1-39 presented for examination. Claims 36-39 are new.

3. Applicant's amendment to the title has been considered and the objection to the title has been withdrawn.

4. Applicant's amendments to claims to overcome 35 U.S.C. 112 2nd have been fully considered and the rejection have been withdrawn.

5. Applicant's amendments to claims 22-31 to overcome 35 U.S.C 101 have been fully considered and the rejection have been withdrawn.

Specification

6. The specification is objected to because of informalities. For example, page 2, last line, "High-end processor 22" should be "High-end processor **20**". Page 7, second to last line, "communication bus 134" should be "communication bus 135". These are examples, the specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-3, 12-14, 22-24,36-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Sexton et al. U.S. Patent No. 5,068,821 (hereinafter Sexton).

9. As per claim 1, Sexton teaches a method of co-processing, comprising:

connecting an interface of a first processor (element 110) to an interface of a second processor (element 120) using a bus, the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing mode (see e.g. Fig. 2. Also, see e.g. col. 5, lines 47-67 to col. 6, lines 1-64); and

sending a task from the first processor to the second processor through the bus, the task comprises an instruction that places the second processor in a slave processing mode (see e.g. col. 5, lines 47-67, wherein the start command is the instruction).

10. As per claim 2, Sexton teaches the invention as claimed above. Sexton further teaches the method of claim 1, wherein the task further comprises an instruction that

places the second processor in a master processing mode (see e.g. col. 5, lines 47-67 to col. 6, lines 1-64).

11. As per claim 3, Sexton teaches the invention as claimed above. Sexton further teaches the method of claim 1, further comprising:

sending data from the second processor to the first processor based on the task received from the first processor (see e.g. col. 5, lines 47-67 to col. 6, lines 1-64).

12. As per claim 12, Sexton teaches an apparatus comprising:

a first processor (element 120) having an interface connected to an interface of a second processor (element 110) using a bus, the interface of the first processor being configurable to place the first processor in a slave processing mode or a master processing mode (see e.g. Fig. 2. Also, see e.g. col. 5, lines 47-67 to col. 6, lines 1-64);

and circuitry, for co-processing (see e.g. Fig. 2, elements 125 and 135), to:

receive a task from the second processor through the bus, the task comprises an instruction that places the first processor in a slave processing mode (see e.g. col. 5, lines 47-67, wherein the first processor (element 120) receives a task (start command) from the second processor (element 110) and places the first processor (element 120) in a slave mode).

13. As per claim 13, Sexton teaches the invention as claimed above. Sexton further teaches the apparatus of claim 12, wherein the task further comprises an instruction

that places the first processor in a master processing mode (see e.g. col. 5, lines 47-67 to col. 6, lines 1-64).

14. As per claim 14, Sexton teaches the invention as claimed above. Sexton further teaches the apparatus of claim 12, further comprising circuitry to:

send data from the first processor to the second processor based on the task received from the second processor (see e.g. col. 5, lines 47-67 to col. 6, lines 1-64).

15. Claims 22-24 are rejected on grounds corresponding to the reasons given above for claims 1-3.

16. As per claim 36, Sexton teaches invention as claimed above. Sexton further teaches wherein the interface of the second processor is configured to provide the task to the second processor when the second processor is in slave mode (see Sexton, e.g. col. 5, lines 47-67 to col. 6, lines 1-64, wherein input port (interface) of the second processor receives the start command, this start command will be sent from the input port (interface) to the second processor), and to send one of a result of the task and another task to the first processor when the second processor is in master mode (see Sexton, e.g. col. 5, lines 47-67 to col. 6, lines 1-64).

17. As per claim 37, it's rejected for the same reasons set forth above in claim 36 except now having the first processor as element 120 and the second processor as element 110.

18. As per claim 38, it's rejected for the same reasons set forth above in claim 36.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 4-10, 15-21, 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sexton in view of Adiletta et al. Intel Technology Journal, Network Processors "The Next Generation of Intel IXP Network Processors" (IDS) hereinafter Adiletta.

21. As per claim 4 and 5, Sexton did not explicitly show the interface of the processors is a quad data rate (QDR) or a media switch fabric. However Adiletta shows using QDR for interface of the SRAM (see e.g. page 10, Fig. 4) and MSF to connect network processors (see page 9-10, section: The media-switch fabric interface), for the

purpose of providing sufficient control information bandwidth for network applications (see e.g. page 11, section: The SRAM cluster. See also page 11, first column).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Adiletta of using QDR or MSF for the interface in the invention of Sexton, for the purpose of allowing the co-processing of Sexton to communicate with the outside world (other network systems or network processors) with sufficient bandwidth (see page 11, section: The SRAM cluster). The advantage of using QDR or MSF is to support high bandwidth applications.

22. As per claim 6, Sexton in view of Adiletta teaches the invention as claimed above. Adiletta further teaches connecting a QDR interface of a processor to an MSF interface of a third processor using a second bus (see e.g. Fig. 2-4). The motivation utilized in the combination of claim 4, super, applies equally as well to claim 6.

23. As per claim 7, Sexton in view of Adiletta teaches invention as claimed above. Sexton in view of Adiletta further teaches the method of claim 6, wherein the first, second and third processors are processors in a plurality of processors and the method further comprises:

connecting the plurality of processors successively in a chain with the first processor at one end of the chain and a last processor at the opposite end of the chain from the first processor, each of the plurality processors having an MSF interface and a

QDR interface (see Adiletta Fig. 4, wherein ME's are plurality of processors. see also the rejection for claim 4-5 above); and

connecting the QDR interface of the last processor to an external memory (see e.g. Fig. 4, DRAMs).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Adiletta in the invention of Sexton, for the purpose of increasing computation capability in the network processor (see Adiletta, e.g. page 13, THE IXP2XXX micro-engine).

24. As per claim 8, Sexton in view of Adiletta teaches invention as claimed above. Sexton in view of Adiletta further teaches the method of claim 7, further comprising:

sending the task from the first processor to the last processor; executing the task; and sending a result to the first processor (see Adiletta, e.g. page 11, 2nd column; page 13, 2nd column to page 16. See also Sexton reference, it also teaches this limitation). The motivation utilized in the combination of claim 7, super, applies equally as well to claim 8.

25. As per claim 9, it is rejected for the same reasons set forth above in claim 7.

26. As per claim 10, it is rejected for the same reason set forth above in claim 8.

27. Claims 15-21 are rejected on grounds corresponding to the reasons given above for claims 4-10.

28. Claims 25-31 are rejected on grounds corresponding to the reasons given above for claims 4-10.

29. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sexton in view of Rajagopal et al. U.S. Patent Application Publication No. 2002/0143998 (hereinafter Raj).

30. As per claim 11, Sexton did not explicitly disclose the processors having different speeds and the first processing speed is greater than the second processing speed. However, Raj shows master and slave processing operate at different speed (see Raj, paragraph [0021]), for the purpose of accommodating different applications within a network.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Raj of allowing varying processing speed in the invention of Sexton, for the purpose of allowing distributing computing environment, and accommodating different applications within a network (see Raj, paragraph [0007]). The advantage of using varying processing speed would significantly utilize the power distribution of the system.

31. Claim 32, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sexton in view of Jungek et al. U.S. Patent Application Publication No. 2002/0009079 (hereinafter Jungek).

32. As per claim 32, Sexton teaches a network router, comprising:

a network co-processing system, the network co-processing system comprising: a first processor having an interface (see Sexton, e.g. Fig. 2, wherein element 110 is the first processor); and

a second processor having an interface connected to the interface of the first processor by a bus (see Sexton, e.g. Fig. 2, wherein element 120 is the second processor), the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing mode (see Sexton, e.g. col. 5, lines 47-67 to col. 6, lines 1-64).

Sexton shows an input line and an output line (see Sexton, Fig. 1, elements 1 and 2). Sexton did not explicitly show the input line connecting to a first network or the output line connecting to a second network. However, Jungek teaches the missing features that Sexton did not teach (see Jungek, e.g. Fig. 9, elements 910 (100A-100B)), for the purpose of allowing intercepting and processing packets communicated between an upstream network and a downstream network.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Jungek in the invention of Sexton, for the purpose of allowing intercepting and processing packets between an

upstream and a downstream networks. The advantage of having an upstream and a downstream would allow the processing elements to perform stateless processing tasks on the up/down packet stream (see Jungek, paragraphs [0190]-[0194]).

33. As per claim 39, Sexton in view Jungek teaches the invention as claimed above. Sexton further teaches the limitation of claim 39 (same reasoning for rejection as in claim 36 above).

34. Claims 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sexton in view of Jungek and further in view of Adiletta.

35. As per claim 33-34, Sexton in view of Jungek did not explicitly show the interface of the processors is a quad data rate (QDR) or a media switch fabric. However Adiletta shows using QDR for interface of the SRAM (see e.g. page 10, Fig. 4) and MSF to connect network processors (see page 9-10, section: The media-switch fabric interface), for the purpose of providing sufficient control information bandwidth for network applications (see e.g. page 11, section: The SRAM cluster. See also page 11, first column).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Adiletta of using QDR or MSF for the interface in the invention of Sexton, for the purpose of allowing the co-processing of Sexton to communicate with the outside world (other network systems or

network processors) with sufficient bandwidth (see page 11, section: The SRAM cluster). The advantage of using QDR or MSF is to support high bandwidth applications.

36. As per claim 35, Sexton in view Jungek and further in view of Adiletta teaches the invention as claimed above. Adiletta further teaches connecting a QDR interface of a processor to an MSF interface of a third processor using a second bus (see e.g. Fig. 2-4). The motivation utilized in the combination of claim 34, super, applies equally as well to claim 35.

Response to Arguments

37. Applicant's arguments filed 02/01/2007 with respect to 35 U.S.C 102(b) have been fully considered but they are not persuasive.

38. The applicant agues "*Thus, it is the bit processor that places itself in master mode (i.e., when the bit processor has control of the resources of the controller 100) or in slave mode (i.e., when the function block processor 110 has control of the resources, such as RAM 135, of Sexton's controller 100). For example, bit processor 120 places itself in master mode in response to a start command written by function block processor 110 (col. 5, lines 56-60). But at no point does sexton describe that an interface of the bit processor 120 or of function block 110 is configured to place the bit processor 120 in master of slave mode. Indeed, Sexton does not even disclose interfaces used in conjunction with either of the processors.*"

The applicant admits "*Sexton bit processor places itself in slave or master mode, for example, bit processor 120 places itself in master mode in response to a start command written by function block processor 110*". The applicant claim recites the same limitation as indicated by Sexton; thus Sexton teaches the limitation of the claim. For example, claim 1 recites "**sending a task from the first processor to the second processor through the bus, the task comprises an instruction that places the second processor in a slave processing mode**." Mapping the teachings of Sexton into the applicant's claim is as follows: "**sending a task from the first processor (***Sexton, Start command written by function block processor 110***) to the second processor through the bus, the task comprises an instruction that places the second processor in a slave processing mode (***Sexton, bit processor 120 places itself in slave mode in response to the start command (task), therefore the start command (task) places the second processor in a slave processing mode***)**."

As for the applicant arguments with respect to the interface "*Indeed, Sexton does not even disclose interfaces used in conjunction with either of the processors.*"

The examiner disagrees, the input/output ports of the processors (Sexton, Fig. 2, element 110 and element 120) are considered equivalent to interfaces. See also Foldoc.org, online computing dictionary (term: interface). Therefore, as the start command reaches the input port of the second processor (Fig. 2, element 120), the input port (interface) sends the start command to the second processor (Fig. 2, element 120) to places it in either slave or master mode.

39. As for applicant's arguments with respect to claims 2-22, the applicant argues "*For reasons similar to those provided with respect to claim 1, Sexton does not disclose or suggest at least the feature of "a second processor having an interface connected to the interface of the first processor by a bus, the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing mode*"

The examiner directs attention to the response to arguments of claim 1 above.

Therefore the argued claims stand as previously rejected.

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

41. The following is text cited from 37 CFR 1.111(c): In amending reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- The I2C-Bus specification is a master-slave protocol. Any connected device has the ability to be the master or slave.
- U.S. Patent No. 7,003,607 shows controllers (bridges) that can be configured to be a master or a slave.
- U.S. Patent No. 6,330,658 shows a master/slave multi-processor arrangement and method thereof.
- U.S. Patent No. 5,835,714 discloses master and slave modes.
- See also attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Idriss N. Alrobaye whose telephone number is 571-270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Idriss Alrobaye

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100